Problem: **Pipelining the DLX Processor (60 points).**  This is the final part of your project assignment. You are to modify DLX Version 1 (dlx1.tg), to create a 3-stage pipelined DLX processor (dlx3.tg).

Note: The starting point of this exercise is either dlx1.tg or the performance-oriented dlx1-fast.tg. Do not start with dlx1-small.tg, since that version is targeted to lower cost, not higher performance.

1. **DLX Processor Version 3 (Pipelined): dlx3.tg**

   Design dlx3, based on a 3-stage pipeline. Try to get as much performance out of your processor as you can with a reasonable amount of effort; you need not try any further once you have achieved a performance of 80 MIPS! You will still receive majority of the credit if you achieve close to 80 MIPS, and properly explain your approach and document any remaining bottlenecks.

**NOTES:**

- Since the focus of this exercise is on speed, you are allowed to ignore circuit size.
- Due to the introduction of a branch-delay slot, you need a different version of the binary code of the GCD assembly program! You will find this code in the file gcd_delay_slot.txt, and its binary version in gcd_delay_slot.bin. Its ROM image is in gcd_delay_slot.rom; you will need to edit system_dlx0.tg to ensure that the processor's ROM is now initialized with the new ROM image.
- Remember that all serious design and optimization work starts with a thorough analysis of the performance of the sub-parts and of possible bottlenecks. At each step, identify the bottleneck and then optimize the design to eliminate it.

Include a block diagram in your report. Include a brief discussion of your method. Explain how you measured the speed in MIPS and motivate that. Present the performance and area numbers as earlier. Keep the entire report brief (5 pages or so).